# THE SYSTEM DESIGN OF 100MHz NEW FREQUENCY STANDARD WITH AN EXCELLENT BEHAVIOR

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## ABSTRACT

The purpose of this paper is to analyze a system which uses a passive quartz resonator as its frequency reference , an assemble system design approach has been proposed which uses both phase–lock and frequency–lock techniques to obtain an optimum transfering of frequency stability of the reference signal by selecting the optimal bandwidth. The phase noise of 100MHz assemble system output can be below −120dB / Hz near carrier 10Hz, the corre sponding frequency stability for sample time over one second can be finally improved to $\sigma_y(\tau) = 2 \sim 3 \times 10^{-13} (\tau \geqq 1s)$. Theoretical analysis and system design on 5MHz frequency–lock loop and 100MHz phase–lock loop have been proposed in this paper, some experimental results have also been given.

## INTRODUCTION

The inherent noise of the best quartz resonator is indeed much lower than that of the crystal oscillator using this resonator. This paper is intended to have an analysis on 100MHz PLL and 5MHz FLLusing quartz resonator as frequency reference. In terms of the given phase noise spectrum of quartz resonator $S_{\varphi r}(f)$, 5MHz VCXO $S_{\varphi q1}(f)$ and 100MHz VCXO $S_{\varphi q2}(f)$, the optimal noise bandwidth for these two loops can be determined,and the output signal can be obtained which has superior frequency stability over a wide range of sample time.

It is estimated that the ultimate performance of the above system can be comparable to that of the $Rb^{87}$maser when sample time is over one second, and the system can also get excellent performance in millisecond–level by a built–in high power low noise crystal oscillator which has an Allan Variance of $\sigma_y(\tau) = 5 \times 10^{-12} / 1ms$. By using phase–lock technigue, the phase noise of 100MHz system output can be below−120dB / Hz near carrier 10Hz.

A simple and effective method of determing the optimal loop bandwidth is to use the given $S_\varphi(f)$ curves in the engineering. The expecting result can be achieved by simulating calculation and experiments.

## 5MHz FREQUENCY LOCK SYSTEM

The system block diagram is shown in Figure 1. Similar to the system scheme of superconducting –cavity stabilized oscillator. The 5MHz crystal oscillator output is phase modulated at 1KHz prior to reflection from the resonator. When the frequency of the incident carrier is close to the resonant frequency

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of the passive quartz resonator, the carrier and phase modulated sidebands are reflected from the resonator. This result to the conversion of some of the incident signal into an amplitude modulated reflected signal which is detected with a low noise square law detector. After AC amplified, the AC–error signal is applied to the synchronous detector, the output of the synchronous detector is a voltage proportional to the difference between the crystal oscillator frequency and the passive resonant frequency. After DC amplifier, filtering, the voltage is fed back to the varactor input of the 5MHz crystal oscillator.

The bandwidth of the quartz resonator at half power is $f_B = f_0 / 2\theta_L$ where $Q_L$ and $f_0$ are quality factor and the center frequency of the quartz resonator respectively.

It can be proved that the above system is an equivalent frequency discrimination serve system which has the following advantages:

1. For the carrier and phase modulated sides travel along the same transmission line, the variation of transmission length has the same effect on carrier and phase modulated sides, after the square law detector, the effection can be compensated.
2. The input signal to square law detector is obtained by the reflection from the quartz resonator instead of the transmission, the modulation frequency can be selected much more than the half bandwidth of the quartz resonator. Thus the feedback gain may be made very large, limited only by noise in electronic components in the loop and drift in DC amplifier.
3. To obtain the best long–term frequency stability, the quartz resonator can work at the optimal power assumption.

We have derived that when carrier frequency $\omega_c$ satisfies $\omega_c - \omega_0 \ll \omega_B$, the AC–error signal is proportional to $(\omega_c - \omega_0)$, the sensitivity of the equivalent frequency discriminator is:

$$S_d = -4aRP_c \frac{V_2}{V_1} \frac{\theta_0}{\theta_0 + \theta_E} \frac{K_{ac}\eta}{f_\theta} \tag{1}$$

Where:

- a is the current sensitivity of the detected diode.
- $P_c$ is the incident carrier power.
- $V_1$ is the incident carrier amplitude.
- $V_2$ is the amplitude of the first pair of the phase–modulated sidebands.
- $\theta_0$ is the unloaded quality factor.
- $\theta_E$ is the external quality factor.
- $K_{ac}$ is the gain of the AC amplifier.
- $\eta$ is the efficiency of the synchronous detector.

If the frequency fluctuation of 5MHz crystal oscillator is taken into account , we can derive that the equivalent frequency discriminator represent a frequency response function of a single–pole low–pass filter to the noise of different frequency. Then the open loop transfer function can be written as:

$$H_0(s) = G_0 D(s) F(s) \tag{2}$$

Where:

$$D(s) = \frac{1}{1 + \frac{s}{\omega_B}} \tag{3}$$

D(s) is called the normalized transfer function for the equivalent frequency discriminator.

F(s) is the transfer function of all other components.

$G_O$ is the overall gain.

In our system, the other electronic components in the serve loop have been designed so the F(s) is mainly determined by the active filter in DC amplifier. The isolation amplifier, preamplifier, and synchronous detector all contribute negligibly to F(s).

The close loop transfer function is :

$$H(s) = \frac{H_0(s)}{1 + H_0(s)} = \frac{G_0 D(s)F(s)}{1 + G_0 D(s)F(s)} \tag{4}$$

Actually, the noise in every components in the loop will have an effect on the output frequency stability. If these effections are considered.We get the equivalent noise model for the serve system which is shown in Figure 2.

In which: $\Delta\omega_{on}$ and $\Delta\omega_{cn}$ represent the frequency fluctuation of the quartz resonator and the crystal oscillator respectively.$Vn_1$ respesent the output noise voltage of the frequency discriminator.$Vn_2$ represent the input noise voltage of the loop filter. $\Delta\omega_{pn}$ and $\Delta\omega_{in}$ represent the frequency fluctuation of the phase modulator and the isolation amplifier respectively.

Since these noise are random and independent from each other. The relative frequency fluctuation of the output signal is determined by the addition of the individual frequency fluctuation.

$$S_{Y_L}(f) = S_{Y_0}(f)|H_L(s)|^2 + [S_{Y_P}(f) + S_{Y_I}(f)]|H_L(s)|^2 + [S_{Vn_1}(f) + S_{Vn_2}(f)] \cdot \left|\frac{K_{dc}K_v F(s)}{1 + s_d K_{dc} K_v D(s)F(s)}\right|^2 + S_{Y_C}(f)\left|H_H(s)\right|^2 \tag{5}$$

where:

$$H_L(s) = \frac{S_d K_{dc} K_v D(s)F(s)}{1 + S_d K_{dc} K_v D(s)F(s)} \tag{6}$$

$$H_H(s) = \frac{1}{1 + S_d K_{dc} K_v D(s)F(s)} \tag{7}$$

From (5) we concluded that the close–loop system has a low–pass filter characteristics to the noise of passive quartz resonator and other loop elements, and a high–pass filter characteristics to the noise of VCXO. So the superior frequency stability of the close–loop system output can be obtained by selecting the optimal loop bandwidth.

## 100MHZ PHASE LOCK SYSTEM

The system block diagram is shown in Figure 3. The VHF voltage controlled oscillator is

phase–locked by an error signal, and the 5MHz FLL output is frequency multiplied by a low noise multiplier and phase detected with a VCXO in quadrature. Such a PLL is designed mainly for improving both the long–term and short–term frequency stability of the VHF VCXO. When the loop is locked. The output signal of VCXO will contain various random phase noise. Of these noises some are from the 5MHz reference sourse $S_{\varphi r}(f)$. Other are caused by the inherent noise of $S_{\varphi q}(f)$, the operational amplifier noise $S_{\varphi ka}(f)$, phase discriminator noise and so on. For simplicy these different noises are added in their corresponding loops respectively. The equivalent noise model of the PLL is shown in Figure 4.

From this noise model, the output signal noise power spectrum can be expressed as:

$$S^{l}_{\varphi q}(f) = [n^2 S_{\varphi r}(f) + S_{\varphi n}(f) + S_{\varphi k_\varphi}(f) + \frac{S_{\varphi ka}(f)}{K_\varphi{}^2}]|H_L(S)|^2 + S^{f}_{\varphi q}(f)|H_H(S)|^2 \tag{8}$$

where $H_L(s)$ is the loop transfer function:

$$H_L(s) = \frac{K_d K_\varphi K_{vco} F(s)}{S + K_d K_\varphi K_{vco} F(s)} \tag{9}$$

$$H_H(s) = 1 - H_L(s) \tag{10}$$

If each element of this loop is carefully designed, its introduced noise can be ignored. The output of the locked crystal oscillator is expressed as:

$$S^{L}_{\varphi q}(f) = n^2 S_{\varphi r}(f)\,|H_L(S)|^2 + S^{f}_{\varphi q}(f)\,|H_H(S)|^2 \tag{11}$$

Supose the noise power spectrum $S_{\Phi r}(f)$ and $S_{\Phi q}(f)$ for the reference sourse and VCXO are given respectively, the optimal loop bandwidth $B_L$of the PLL can be obtained by graphic method. Generally, we consider the crosspoint of the two curves $S_{\varphi r}(f)$ and $S_{\varphi q}(f)$ as the optimal value of $\omega_n$. In our system, two–order active filter is adopted and the loop parameters $R_1$, $R_2$, $R_F$, C and $K_F(o)$ can be easily calculated.

At present, the noise power spectrum of 5MHz quartz resonator $S_{\varphi r}(f)$, 5MHz VCXO $S_{\varphi q1}(f)$, and 100MHz VCXO $S_{\varphi q2}(f)$ can be made:

$$S_{\varphi r(f)} = 2 \times 10^{-13} f^{-3} + 10^{-19.0} f^{-2}$$

$$S_{\varphi q1}(f) = 10^{-10.3} f^{-3} + 10^{-17.4}$$

$$S_{\varphi q2}(f) = 10^{-6.8} f^{-3} + 10^{-12.0} f^{-1} + 10^{-16.0}$$

Using the above FLL and PLL serve system, and the loop elements being low noise designed, the phase noise of 100MHz system output near carrier 10Hz can be expected below −120dB / Hz, and −137dB / Hz near carrier 100Hz , the background noise remains −160dB / Hz.

Now, both 5MHz FLL and 100MHz PLL system have been developed in our institute, and all the loop elements in these two serve system are made by ourself. Experiments showed that the above system approach is visible, and the long term frequency stability of the 100MHz output signal can be finally improved by a factor of 100. The short–term frequency stability can be made to $\sigma_y(\tau)$: $2 \sim 3 \times 10^{-13}(\tau \geqq 1s)$, $3 \times 10^{-11}(\tau = 1ms)$.Further research work is going to be done.

## CONCLUSION

An assemble system design approach has been proposed which uses both phase lock and frequency lock technigues to obtain an optimal transfering of frequency reference.So that the output frequency of this system would have an excellent behavior within a large extent.

The ultimate performance of such a system is to have a good frequency stability for sample time from 1ms to 100s. A simple and effective method of determing the optimal loop bandwidth is to use the given $S_{\varphi}(f)$ curves in the engineering.The expecting result can be achieved by simulating calculation.

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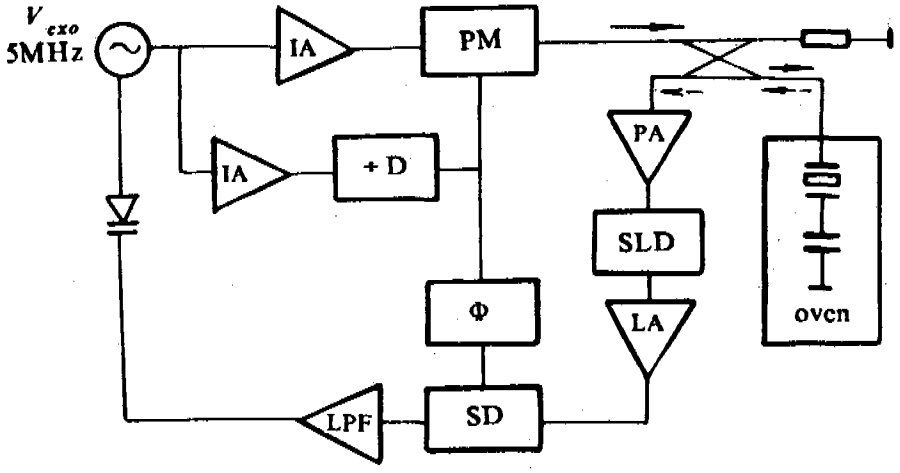


Figure 1. Block diagram of 5 MHz frequency lock system

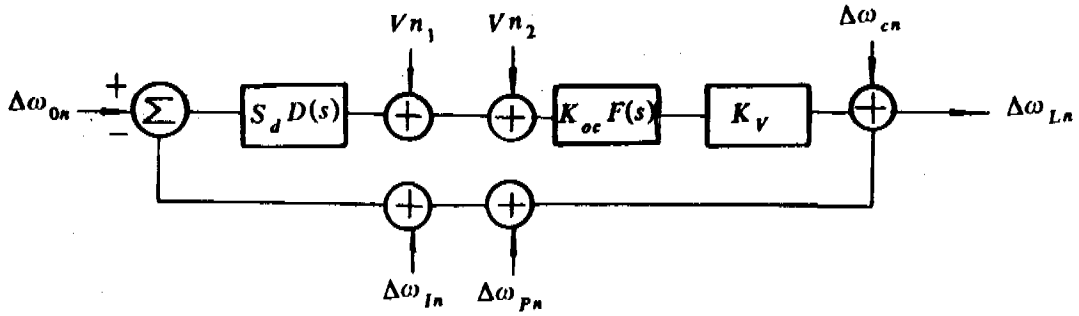


Figure 2. Equivalent noise model of 5MHz FLL system

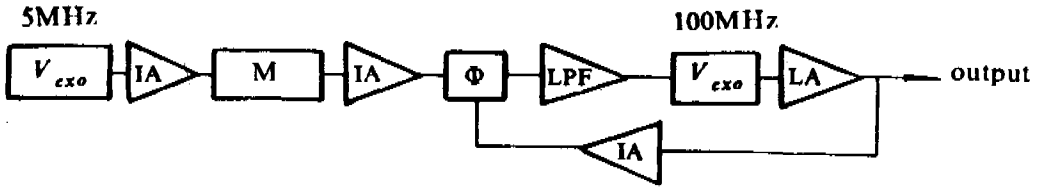


Figure 3. Block diagram of 100MHz phase–lock system

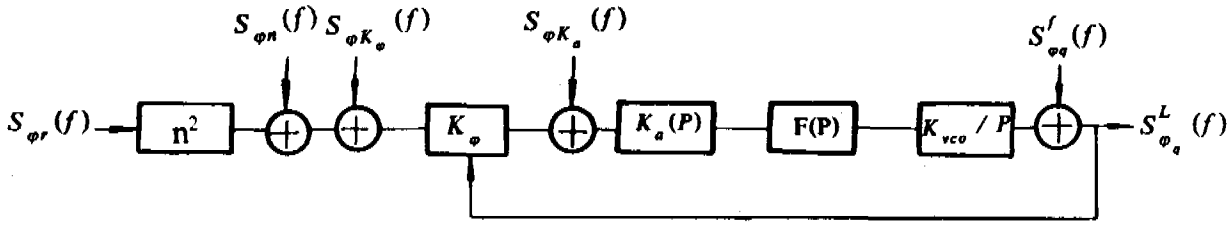


Figure 4. Equivalent noise model of 100MHz PLL system